

Amendments to the Claims

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Currently Amended) Circuit testing equipment for testing a circuit that has at least one first integrated circuit (IC) that is boundary-scan capable and at least one second IC that is not boundary-scan capable, and in particular for testing interconnections between the first IC and the second IC, the equipment comprising:

a computer having stored thereon a boundary scan description language (BSDL) file for the first IC, and a netlist and a connections list for the circuit to be tested, and having loaded therein a test script specific to the second IC, for testing the second IC; and

a connector for connecting the computer to a boundary scan bus of a circuit to be tested;
the computer being arranged to parse the BSDL file, the netlist and the connections list,
to find points from which selected pins of the second IC can be driven and read via the first IC,
and to generate a data structure therefrom which, ~~when combined with a test script,~~ permits automated execution of the test script from the computer through the boundary scan bus whereby the interconnections between the first IC and the second IC can be tested.

2. (Currently Amended) The equipment of claim 1 for testing a connection to a first pin of a
~~first device~~the second IC of the circuit to be tested, wherein the computer has all information
necessary to identify ~~whether, for a given pin, a BSDL file is present and whether the first given~~
pin is connected through the netlist to a second pin of a device~~the first IC~~ for which a BSDL file
is present, whereby the first pin can be controlled using the boundary scan bus.

3. (Currently Amended) [Equipment] The equipment according to claim 1, wherein the
computer comprises a parser for parsing the BSDL file, the netlist and the connections list, and a
compiler for compiling the same to generate the data structure for execution with the test script.

4. (Cancelled)

5. (Currently Amended) [Equipment] The equipment according to claim 41, ~~for testing a circuit that has at least one boundary scan capable IC, the at least one boundary scan capable IC having at least a first pin and a second pin, wherein the second IC has pins that are at least the first pin is capable of adopting one of three states, being a high state, a low state and an input state, and wherein the test script is arranged to sequentially test whether a pin is in a read state by testing whether it can sequentially be driven into the low state and the high state~~

~~the equipment further comprising connection test software arranged to test that the first and second pins are not connected, by setting the first pin to the input state and driving the second pin sequentially into the high and low states.~~

6. (Currently Amended) [Equipment] The equipment according to claim 1, wherein the computer further comprises a first test script for testing a first integrated circuit of the circuit to be tested and a second test script for testing a second integrated circuit of the circuit to be tested.

7. (Currently Amended) Circuit testing equipment ~~according to claim 1~~ for testing a circuit that has at least one first integrated circuit (IC) that is boundary-scan capable and at least one second IC that is not boundary-scan capable and in particular for testing interconnections between the first IC and the second IC, comprising:

a computer having stored thereon a boundary scan description language (BSDL) file for the first IC, and a netlist and a connections list, for the circuit to be tested and having loaded therein a test script specific to the second IC for testing the second IC; and

a connector for connecting the computer to a boundary scan bus of the circuit to be tested;

the computer being arranged to parse the BSDL file, the netlist and the connections list, to find points from which selected pins of the second IC can be driven and read via the first IC,

and to generate a data structure therefrom which wherein the data structure defines all pins of the first IC that are capable of driving pins of the second IC and all pins of the first IC that are capable of reading pins of the second IC, which permits automated execution of the test script from the computer through the boundary scan bus, whereby the second IC and its connections to the first IC can be tested through the boundary scan bus by driving pins of the first IC.

8. (Currently Amended) Circuit testing equipment for testing a circuit that has at least one first integrated circuit (IC) that is boundary-scan capable, and at least one second IC that is not boundary-scan capable, the equipment comprising:

an input for inputting files comprising a boundary scan description language (BSDL) file for the first circuit, and a netlist and a connections list, for the circuit to be tested; and

a data structure generated ~~from~~ by parsing of the BSDL file, the netlist and the connections list to find points from which selected pins of the second IC can be driven and read via the first IC, wherein the data structure that defines all pins of the first IC that are capable of driving pins of the second IC and all pins of the first IC that are capable of reading pins of the second IC, whereby the second IC and its connections to the first IC can be tested by driving pins of the first IC using a test script that is specific to the second IC but independent of the first IC, the netlist and the connections list.

9. (Original) Equipment according to claim 7 wherein the first IC has pins that are capable of adopting one of three states, being a high State, a low state and an input state.

10. (Original) Equipment according to claim 7 wherein the first IC is connected to a boundary scan bus.

11. (Original) Equipment according to claim 7, further comprising a parser and a compiler for parsing and compiling the BSDL file, the netlist and the connections list to generate the data structure, wherein the parser and compiler are implemented in computer programs loaded into a computer to be connected to the circuit to be tested.

12 (Currently Amended). Equipment according to claim 11, wherein the computer further comprises a test script for testing the second IC and independent of its connections to the first IC.

13. (Currently Amended) [Equipment] The equipment according to claim 8, wherein the at least one first IC has at least a first pin and a second pin, wherein at least the first pin is capable of adopting one of three states, being a high state, a low state and an input state,

the equipment further comprising connection test software arranged to test that the first and second pins are not connected, by setting the first pin to the input state and driving the second pin sequentially into the high and low states.

14. (Canceled)

15. (Canceled)

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

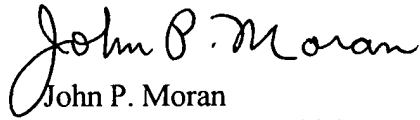
21. (Canceled)

22. (Canceled)

23. (Newly Added) The circuit testing equipment according to claim 1, wherein the test script is also associated with other electrical components to be tested, including at least one of switches and light emitting diodes.

If any additional fee is required in connection with this Preliminary Amendment, Applicants requests that such fee be charged to Deposit Account No. 502353.

Respectfully submitted,,

A handwritten signature in black ink that reads "John P. Moran". The signature is fluid and cursive, with the first letters of each word being capitalized and prominent.

John P. Moran
Registration No. 30,906
Holland & Knight LLP
2099 Pennsylvania Ave., NW; Suite 100
Washington, D.C. 20006
Telephone: 202-828-1848
Facsimile: 202-955-5564

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